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JUL 23 2007

REMARKS

Prior to the present amendment and response, claims 1-9 were pending in the present application. By the present amendment, claims 1 and 2 have been amended, and claims 10-15 are canceled in confirmation of a previous restriction requirement. Thus, claims 1-9 remain in the present application. Reconsideration and allowance of outstanding claims 1-9 in view of the above amendments and the following remarks are requested.

A. Election without traverse

The Examiner has stated that Applicants' failure to specifically rebut the grounds upon which the Examiner's previous restriction requirement was based have resulted in election without traverse of elected claims 1-9 in the present application. Applicants herein accept the Examiner's assertion with respect to election, and affirm election of claims 1-9, and non-election of claims 10-15, without traverse. As a result, Applicants hereby confirm the election made without traverse and cancel claims 10-15.

B. Objection to drawings under 37 CFR 1.83(a)

The Examiner has objected to the drawings under 37 CFR 1.83(a). The gist of the Examiner's objection seems to be a lack of concordance between claim language reciting a "plurality of core stacks, plurality of source regions and plurality of drain regions," and Figure 2, which shows only a single example of each (Non-final Office Action of April

24, 2007, page 2, item 3). As an alternative to amending the drawings, Applicants herein respond to the Examiner's objection by amending claims 1 and 2 to correspond to the original drawings, while acknowledging their exemplary nature, by referring instead to "at least one core stack, at least one source region, and at least one drain region," as is shown in Figure 2 (Currently amended claims 1 and 2). As a result of the current amendments to claims 1 and 2, Applicants respectfully assert that all presently pending claims correspond to the drawings as originally submitted, and consequently request that Examiner withdraw the objection to the drawings.

C. **Rejection of claims 1-9 under 35 USC §102(b)**

The Examiner has rejected claims 1-9 under 35 USC §102(b) as being anticipated by U.S. Patent Number 5,780,891 to Kauffman et al. ("Kauffman"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by independent claim 1, is patentably distinguishable from Kauffman.

The present invention, as defined by independent claim 1, is directed to a flash memory device structure possessing the advantages associated with incorporation of an anti-reflective material, without the drawbacks flowing from the additional processing steps required by use of an anti-reflective coating. Including an antireflective layer in a flash memory device structure may advantageously improve image formation during lithographic patterning. As explained in the present disclosure, during production of a flash memory device, an anti-reflective material can be "used to cut down on light

scattering from a surface into a resist mask." (The present application, page 1, lines 24-25.) Thereby providing "superior patterning" and improved definition of small images. (*Id.* at line 26.) "In addition, anti-reflective coatings minimize standing wave effects, such minimization improving the image contrast." (*Id.* at lines 26-28.)

As Applicants further disclose, conventional approaches to achieving the patterning advantages described, utilize an anti-reflective coating formed over a second polysilicon layer serving as a control gate on a core stack. (*Id.* at page 2, lines 3-7.) However, because conventional approaches obtain the image patterning advantages derived from inclusion of an anti-reflective material, by implementing it as an anti-reflective coating "placed on the top of core stacks," additional processing steps are required. (*Id.* at lines 1-2.)

Applicants achieve substantially the same benefits of utilizing an anti-reflective coating through an entirely novel approach to introducing an antireflective material between polysilicon layers used to form a core stack in a flash memory device. As a result, Applicants obtain the image patterning advantages of including an antireflective material, while avoiding the additional processing steps required by its implementation as a coating. Applicant's approach calls for implementation of the anti-reflective material, not as a coating, but as an anti-reflective interpoly layer. Applicants' single anti-reflective layer, disposed between first and second polysilicon layers utilized respectively as field and control gates, acts both to prevent reflection during lithographic patterning,

and to provide the electrical insulation necessary for proper functioning of the resulting device as a flash memory stack.

The intent of Applicants to provide a device comprising a single interpoly layer with anti-reflective properties may be seen from independent claim 1, which recites, in part, the following elements: "(2) a first polysilicon layer on the tunnel oxide layer; (3) *an* anti-reflective interpoly layer *on* the first polysilicon layer; and (4) a transmissive second polysilicon layer *on* the anti-reflective interpoly layer; . . ." (Currently amended independent claim 1, *italics added for emphasis*.) Applicants' choices of indefinite article and preposition, italicized in the foregoing quote, are unambiguous in describing a structure having a single interpoly layer in contact with both a first polysilicon layer and a second polysilicon layer, with no additional layers interposed. Applicants believe that this novelty sets the invention distinctively apart from conventional implementations, including the disclosure provided by Kauffman.

In contrast to the present application's disclosure and claims, Kauffman expresses no interest in the image patterning advantages associated with including an anti-reflective material in a flash memory core stack. Instead, Kauffman's focus is on preserving high capacitance and high leakage current resistance as the dimensions of flash memory devices are reduced. According to Kauffman:

> As the cell spacing of floating gate memory devices is reduced, a very high quality interpoly dielectric is needed to maintain a high specific capacitance between the floating gate and the control gate. This dielectric must perform effectively during the application of high charging voltages and also prevent leakage between the floating gate and the control gate after charging. (Kauffman, column 1, lines 48-53.)

Thus, while Kauffman states that "it is *critical* that leakage between the floating gate and the control gate be minimized," no interest is expressed in achieving the benefits for image contrast and small pattern resolution central to the present application's disclosure. (*Id.* at lines 54-56.)

Kauffman's indifference to image patterning is further evidenced by the asserted objects of the invention disclosed there. Again, according to Kauffman:

> One object of the invention is to provide a floating gate memory having a high specific capacitance between the floating gate and the control gate, even at reduced cell spacing on the order of 1.0 micron. It is another object of the invention to provide a floating gate memory in which the specific capacitance and leakage resistance between the floating gate and the control gate is very high. It is another object of the invention to provide a method for fabricating a floating gate memory in which the interpoly dielectric has a uniform thickness. (*Id.* at column 2, lines 12-23.)

As can be seen from the foregoing, nowhere does Kauffman indicate that anti-reflective properties or their effect on image patterning are either direct or indirect objectives of the invention being disclosed.

Kauffman's disclosure goes on to reveal that its own objectives are achieved through introduction of a multi-layer film stack – including at least a silicon oxide layer underlying a silicon oxynitride layer – between a floating gate and a control gate. (*Id.* at column 4, lines 33-50.) Kauffman is explicit in distinguishing its approach from those merging a variety of materials into an effective single interpoly layer, stating unequivocally: "In the present invention, by contrast, the oxynitride film is a separate and

distinct compound deposited *over the underlying layer of silicon dioxide.*" (*Id.* at column 2, lines 47-50, *italics added for emphasis.*)

Thus, while the present application seeks to obtain the image patterning advantages derived from inclusion of an antireflective material as a single interpoly layer in a flash memory core stack, Kauffman seeks instead to optimize the dielectric properties of an interpoly region by introducing a stack of discrete film layers in that region. The present application discloses and claims its single anti-reflective interpoly layer as being "on a first polysilicon layer," and having a second polysilicon layer "on" it (Currently amended independent claim 1). Kauffman, by contrast, discloses only formation of a silicon dioxide layer on a first polysilicon layer, followed by deposition of an oxynitride layer over the silicon dioxide layer. (Kauffman, column 3, line 60 through column 4, line 3.) In other words, Kauffman does not disclose an anti-reflective layer alone, nor does it disclose an anti-reflective layer in direct contact with a first polysilicon layer. This is unsurprising, however, considering that for Kauffman preventing leakage between the first and second polysilicon layers is the critical objective. Consequently, it may be seen that the present application discloses and claims a structure comprising an implementation, i.e. disposition of a single anti-reflective interpoly layer on a first polysilicon layer, distinct from that disclosed in Kauffman, in order to achieve objectives, i.e. advantageous image contrast and small pattern resolution, ignored by Kauffman.

For the foregoing reasons, Applicants respectfully submit that the present invention, as defined by currently amended independent claim 1 is patentably novel and

inventive over Kauffman. As a result, claims 2-9, depending from independent claim 1, are also patentably novel and inventive over Kauffman for the additional limitations contained in each dependent claim. It is noted that dependent claim 2 is herein amended merely to conform to the amendments introduced to independent claim 1.

D. Conclusion

Based on the foregoing reasons, the present invention, as defined by currently amended independent claim 1 and claims depending therefrom, is patentably novel and inventive over the art cited by the Examiner. Moreover, Applicants assert that no new matter has been introduced herein. Thus, for all of the reasons presented above, an early allowance of claims 1-9 pending in the present application is respectfully requested.

Attorney Docket No.: 0180221

Respectfully Submitted,
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Dated: 7/23/07

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